happening. As the cuts 92 are made through the panel stack 66, portions of the panel 32 hold the chip package stacks 10 together in strips of four, as shown in FIG. 8. The strips can then simply be flexed so as to break the joining portions of the panel 32 along the scores 40 thereof so as to separate the individual chip package stacks 10 from each other within the strips.

As noted, routing or other cutting of the panel stacks 66 along the cut lines 92 separates the panel stacks 66 into strips of the chip package stacks 10. One such strip 96 is shown in FIG. 8. The strip 96 is comprised of four chip package stacks 10 held together by the interconnecting portions of the topmost panel 32 which remain after the cutting is done. As shown in FIG. 8, the slots 48 in the panels 34 act to separate the chip package stacks 10 when the cuts 92 are made. However, the routing used to perform the cuts 92 does not completely separate the chip package stacks 10 within each strip 96 because of the scored interconnecting portions of the uppermost panel 32. By then flexing the chip package stacks 10 relative to each other and to remaining end portions 98 at the opposite ends of the strip 96, the interconnecting portions of the uppermost panel 32 are snapped or broken along the scores 44 and 46 therein to separate the chip package stacks 10 of the strip 96, as shown in FIG. 1.

Referring again to FIG. 2, and in a final step 100, the chip package stacks 10 separated from the panel stack 66 by the cutting and breaking step 90 are cleaned to remove any debris or residue that may remain from the step 90 or from earlier steps in the process. As in the case of the step 88, the cleaning can be carried out using an aqueous cleaning system with a mild detergent.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

We claim:

1. A method of making chip stacks comprising the steps of:

providing a plurality of panels, each having a plurality of apertures therein and a plurality of conductive pads thereon;

providing a plurality of packaged chips having leads extending therefrom;

mounting the plurality of packaged chips within the plurality of apertures in the plurality of panels so that the leads thereof are disposed on at least some of the plurality of conductive pads on the plurality of panels;

assembling the plurality of panels into a panel stack;

soldering the leads of the packaged chips to at least some of the plurality of conductive pads and at least some of the conductive pads on adjacent panels together to form chip package stacks within the panel stack; and

separating the individual chip package stacks from the panel stack;

wherein one of the plurality of panels is scored to facilitate breaking of the panel between adjacent chip package stacks, and the remaining ones of the plurality of panels have elongated slots therein to facilitate separation of adjacent chip package stacks; and

wherein said one of the plurality of panels is scored along a plurality of spaced-apart, parallel score lines which

are perpendicular to the elongated slots in said remaining ones of the plurality of panels, and the step of separating the individual chip package stacks includes the steps of cutting through the panel stack along a plurality of spaced-apart, parallel lines which are perpendicular to the score lines, to form a plurality of strips of the chip package stacks, and within each strip breaking the strip along the score lines of a portion of said one of the plurality of panels within the strip to separate the individual chip package stacks from the strip.

2. A method of making chip stacks comprising the steps of:

providing a plurality of thin, planar panels, each having a plurality of apertures therein, a plurality of conductive pads on opposite surfaces of the panel adjacent each of the plurality of apertures, and a plurality of slots therein on opposite sides of each of the plurality of apertures;

mounting a different one of a plurality of packaged chips having leads within each of the plurality of apertures of each of the plurality of panels;

assembling the plurality of panels into a panel stack;

bonding the leads of the plurality of packaged chips to at least some of the plurality of conductive pads of the panels on which the packaged chips are mounted, and bonding at least some of the plurality of conductive pads of each panel to at least some of the conductive pads on at least one adjacent panel of the plurality of panels to form chip package stacks within the panel stack; and

cutting through each of the plurality of panels within the panel stack along lines perpendicular to the plurality of slots in each of the panels to separate the chip package stacks from the panel stack.

3. The method set forth in claim 2, wherein one of the plurality of thin, planar panels is formed without the pluralit of slots therein and is broken following the cutting step to separate the chip package stacks.

4. The method set forth in claim 2, wherein the plurality of apertures in each panel are arranged into columns thereof extending along a length of the panel and rows thereof extending across a width of the panel and the plurality of slots in the panel are located between adjacent rows of the apertures.

5. The method set forth in claim 4, wherein the step of cutting is performed by cutting through each panel of the panel stack along the length of the panel adjacent opposite sides of the columns of apertures.

6. The method set forth in claim 2, wherein each of the plurality of apertures in each of the panels is of rectangular configuration so as to have four side edges which are surrounded by the conductive pads on each of the opposite sides of the panel, and each of the packaged chips comprises a thin, small outline chip package of rectangular configuration having plural leads extending from a pair of opposite side edges of the package and onto the conductive pads adjacent an opposite pair of side edges of an aperture in which the chip package is mounted, the chip package having a thickness like a thickness of the panel between opposite sides of the panel.

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